

REMARKS

Claim 1-14, 15-17, and 19-27 are pending in the application. Claims 1, 4, 9-11, 13, 15-16, 19-21, and 23-26 have been amended, and claims 14 and 18 have been cancelled. Further, claim 27 has been newly added. No new matter has been introduced by the amendment.

Claim Objection

Claim number 25 appeared twice in the applicants' claims following entry of the Preliminary Amendment submitted with the application. This inadvertent error has been corrected in the Listing of Claims included herewith. The second instance of claim number 25 has been changed to claim number 26.

Rejection Under 35 U.S.C. §103(a)

Claims 1-26 have been rejected over the Background section of the applicants' specification in view of Joly et al. This rejection is overcome in view of the amendment of the claims together with the following remarks.

Claim 1, as amended, recites a method in which an interconnection line is produced after bonding the first and second substrates. The second substrate includes critical passive components and the interconnection line passes through the second substrate. The interconnection line is produced after bonding the first and second substrates. The claimed interconnection line is shown, for example, in FIG.4 of the applicants' drawing, and described in pages 12 and 13 of the applicants' Substitute Specification. As noted in the applicants' specification, placing the inductors away from the bonding face reduces induced current losses. (See, pg. 14. II. 4-8). The applicants assert that their claimed method is not suggested or disclosed by either Joly et al. or the background section of their specification.

The process disclosed by Joly et al. differs from claim 1 in that Joly et al. deposit successive layers on a substrate. An active component is formed in a lower layer and a passive component is subsequently-formed in an upper layer. An electrical connection is formed in the layer containing or overlying the active component. An insulating substrate is then bonded to the layer containing the passive component. The substrate upon which the layers are formed is then eliminated by grinding, etching, or polishing. (Col. 6, ll. 10-15, Col 7, ll. 3-6 and ll. 31-37). Joly et al. do not suggest or disclose forming an interconnection line that passes through the second substrate after bonding the first and second substrates, as recited in claim 1.

The applicants assert that the addition of the background section of their specification does not overcome the deficiency of Joly et al. In their background section, the applicants describe various solutions disclosed in the prior art to diminish disturbance effects. With respect to methods for reducing induced current caused by inductors and conductive lines, the applicants describe three known prior art solutions on page 5 of their Substitute Specification. One is to eliminate a portion of the substrate under areas in which inductors and conductive lines are formed. Another is to form insulation in areas that receive conductors and inductors. Yet another is to structure the underlying layers in a checkerboard pattern. Accordingly, none of the disclosed prior art references suggest or disclose the method recited in claim 1.

Claims 2-13 are allowable in view of their direct or indirect dependence from claim 1. Also, claims 4 and 13 have been amended to improve their form. Further, claims 9-10 have been amended to change their dependence to claim 1, and the dependence of claim 11 has been changed from claim 9 to claim 10.

Claim 15 recites a die formed by the process of claim 1. Further, claim 16, as amended, recites a die including a single stack of layers. A first portion of the die resides on one side of an interface that includes at least one active component. A

second portion includes critical passive components, and at least one interconnection line between the components of the first and second portions that passes through the second portion. The applicants assert that neither Joly et al. nor the background section of their specification suggest or disclose the die recited in claims 15 and 16.

The final structures obtained by the disclosed processes of Joly et al. are illustrated in FIGs. 1G, 2D, 3E, and 4B. None of the final structures suggest or disclose a die having an interface and a first portion on one side of the interface and a second portion including critical passive components, where at least one interconnection line between the components of the first and second portions that passes through the second portion. Instead, all of the embodiments disclosed by Joly et al. show an electrical interconnect extending through a dielectric layer that either includes the active component (1) and (21), or overlies the active component. Accordingly, the bonding interface is away from and opposite the passive components (3) and (24), rather than between the passive and active components, as in the applicants' die.

Claims 17 and 19-26 are allowable in view of their direct or indirect dependence from claim 16.

Claims 19, 25, and 26 have been amended to improve their form and the dependence of claims 20-21, 23, and 25 has been changed to claim 16. Further, the dependence of claim 24 had been changed from claim 22 to claim 23.

New Claim

Claim 27 is newly added and recites that the interconnection line and at least one inductor are produced during the same processing step. Support for claim 27 can be found, for example, at page 13, lines 14-31 of the applicants' specification.

This claim is not suggested or disclosed by either Joly et al. or the background section of the applicants' specification.

The applicants have made novel and non-obvious contribution to the art of integrated circuits including active and passive components and to their fabrication. The claims at issue are distinguished over the cited references and are in condition for allowance. Accordingly, such allowance is now earnestly requested.

Respectfully submitted,

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